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8

9              UNITED STATES DISTRICT COURT

10           NORTHERN DISTRICT OF CALIFORNIA

11                 SAN JOSE DIVISION

12  VERIGY US, INC, a Delaware Corporation          Case No. C07-04330 RMW (HRL)

13                        Plaintiff,               **DECLARATION OF KEN HANH DUC
                                                   LAI IN SUPPORT OF PLAINTIFF'S
14        vs.                                      REPLY AND SUPPLEMENTAL BRIEF
                                                   RE ORDER TO SHOW CAUSE RE
15  ROMI OMAR MAYDER, an individual;               PRELIMINARY INJUNCTION**
    WESLEY MAYDER, an individual; SILICON
16  TEST SYSTEMS, INC., a California Corporation;   Date:  December 14, 2007
    and SILICON TEST SOLUTIONS, LLC, a             Time:  9:00 a.m.
17  California Limited Liability Corporation,       Place: Courtroom 6
    inclusive,                                      Judge: Hon. Ronald M. Whyte
18
                                                   
19                        Defendants.              Complaint Filed:    August 22, 2007
                                                   Trial Date:         None Set
20

21

22

23          **HIGHLY CONFIDENTIAL – ATTORNEYS EYES ONLY**

24              **DOCUMENT SUBMITTED UNDER SEAL**

25

26

27

28

DECLARATION OF KEN HANH DUC LAI
CASE NO. C07-04330 RMW (HRL)

1      I, Ken Hanh Duc Lai, declare as follows:

2      1.     I make this declaration of my personal knowledge and, if called as a witness, I

3 could and would testify competently to the facts set forth herein.

4      2.     The document attached as Exhibit A to my previous declaration called

5 ███████████████████████ is a document I created that includes ████████

6 ████████████████████████████████████████████

7 ████████████. For example, in the ████████████████

8 ████████████████████████████████████████████

9 ████████████████████████████████████████

10 ████████████████████████████ I created based on the ████████

11 (attached as Exhibits B-D to my previous declaration) were intended as rough draft documents to

12 be incorporated in other Verigy documents. For example, the ████████████████

13 ████████████████████████████████████████

14 ████████████████████████████████ A true and correct

15 copy of the Boreal ███████████████ is attached hereto as Exhibit 1.

16      3.     Because the ████████████ (Exhibits A-D to my previous declaration)

17 were intended as rough draft documents, they were not marked "confidential," but I treated them

18 as such and it is my understanding and belief that the other Verigy employees who had access to

19 these documents treated them as confidential as well. The ██████████████████

20 ██.

21      4.     The ████████████ as Exhibits B-D to my previous declaration, also include

22 much information that would not be available ████████████████

23 ████████████████████████████████████████

24 ████████████████████████████████████████

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26 ████████████████████████████████████████

27 ████████████████████████████████████████

28 ████████████████ Attached hereto as Exhibit 2 is a true and correct copy of a

DECLARATION OF KEN HANH DUC LAI
CASE NO. C07-04330 RMW (HRL)

1  Hynix NAND data sheet downloaded from the Hynix website at www.hynix.com. Exhibit 2 does

2  not disclose

3      5.    I am also the author of another

4                                              ." A true and correct copy of this document is

5  attached hereto as Exhibit 3. This document went through numerous revisions and was also

6  created as a rough draft           with information to be incorporated in other Verigy

7  documents. In fact,                                                            and

8  marked "Verigy restricted" has placeholders on pages 17 through 26 for me to insert this

9  information. This document currently includes figures from an earlier version

10                                                                                      ;

11                  A true and correct copy of the June 6, 2006 Boreal DEF Checkpoint is

12  attached hereto as Exhibit 4.

13      6.    Again, this                      was a rough draft document, and therefore it was

14  not marked "confidential." However, I treated it as confidential and the content in this document

15  is clearly proprietary information, including details related to

16

17                                      It is my understanding and belief that the other Verigy

18  employees who had access to these documents treated them as confidential as well. This

19  document was stored in the

20      I declare under penalty of perjury under the laws of the United States that the foregoing is

21  true and correct.

22      Executed this 14 day of November, 2007 in Cupertino, California.
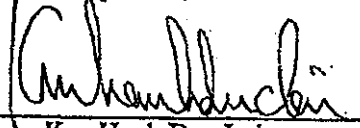
23

24

25                                  Ken Hanh Duc Lai

26

27

28

2

# EXHIBIT 1
## TO LAI DECLARATION

# HIGHLY CONFIDENTIAL – ATTORNEYS EYES ONLY

# EXHIBIT FILED UNDER SEAL

# EXHIBIT 2

**hynix**

**HY27US(08/16)12(1/2)B Series**
**512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**

# 512Mb NAND FLASH
## HY27US(08/16)12(1/2)B
## HY27US0812(1/2)B
## HY27US1612(1/2)B

**hynix**

## Document Title
512Mbit (64Mx8bit / 32Mx16bit) NAND Flash Memory

## Revision History

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | Initial Draft. | Oct. 19. 2006 | Preliminary |
| 0.1 | 1) Correct Figure 14 & 15 | Mar. 07. 2007 | |
| 0.2 | 1) Add AC Characteristics<br>- tRB : Last $\overline{RE}$ High to busy (at sequential read)<br>- tCRY : $\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at read)<br>- tCEH : $\overline{CE}$ High Hold Time (at the last serial read) | Mar. 26. 2007 | |
| 0.3 | 1) Add sequential row read feature and figure<br>2) Modify Block Replacement | Apr. 27. 2007 | |
| 0.4 | 1) Add x16 Characteristics<br>2) Modify read2 operation (sequential row read)<br>3) Add AC Characteristics<br>- tOH : $\overline{RE}$ or $\overline{CE}$ High to Output Hold | May. 29. 2007 | |
| 0.5 | 1) Correct Read ID Table 16<br>2) Correct System Interface Using CE don't care operation<br>3) Correct Command Set Table 5 | Jul. 20. 2007 | |

# hynix

**HY27US(08/16)12(1/2)B Series
512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**

## FEATURES SUMMARY

### HIGH DENSITY NAND FLASH MEMORIES

- Cost effective solutions for mass storage applications

### NAND INTERFACE

- x8 or x16 bus width.
- Multiplexed Address/ Data
- Pinout compatibility for all densities

### SUPPLY VOLTAGE

- VCC = 2.7 to 3.6V  : HY27US(08/16)12(1/2)B

### Memory Cell Array

x8 :  (512+16) Bytes  x 32 Pages x 4,096 Blocks

x16 :  (256+8) Words  x 32 Pages x 4,096 Blocks

### PAGE SIZE

- x8 device  : (512+16) Bytes

           :  HY27US0812(1/2)B

- x16 device  : (256+8) Words

           :  HY27US1612(1/2)B

### BLOCK SIZE

- x8 device: (16K + 512 spare) Bytes
- x16 device: (8K + 256 spare) Words

### PAGE READ / PROGRAM

- Random access: 12us (max.)
- Sequential access: 30ns (min.)
- Page program time: 200us (typ.)

### COPY BACK PROGRAM MODE
- Fast page copy without external buffering

### FAST BLOCK ERASE
- Block erase time: 2ms (Typ.)

### STATUS REGISTER

### ELECTRONIC SIGNATURE

- 1st cycle: Manufacturer Code
- 2nd cycle: Device Code

### CHIP ENABLE DON'T CARE

- Simple interface with microcontroller

### HARDWARE DATA PROTECTION

- Program/Erase locked during Power transitions

### CE DON't CARD OPTION ONLY

### DATA RETENTION
- 100,000 Program/Erase cycles (with 1bit/512byte ECC)
- 10 years Data Retention

### PACKAGE
- HY27US(08/16)12(1/2)B-T(P)
       : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
        - HY27US(08/16)12(1/2)B-T (Lead)
        - HY27US(08/16)12(1/2)B-TP (Lead Free)

- HY27US0812(1/2)B-S(P)
       : 48-Pin USOP1 (12 x 17 x 0.65 mm)
        - HY27US0812(1/2)B-S (Lead)
        - HY27US0812(1/2)B-SP (Lead Free)

- HY27US0812(1/2)B-F(P)
       : 63-Ball FBGA (9 x 11 x 1.0 mm)
        - HY27US0812(1/2)B-F (Lead)
        - HY27US0812(1/2)B-FP (Lead Free)

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**HY27US(08/16)12(1/2)B Series**
**512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**

## 1. SUMMARY DESCRIPTION

The Hynix HY27US(08/16)12(1/2)B series is a 64Mx8bit with spare 2Mx8 bit capacity. The device is offered in 3.3V Vcc Power Supply.

Their NAND cell provides the most cost-effective solution for the solid state mass storage market.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The memory contains 4096 blocks, composed by 32 pages consisting in two NAND structures of 16 series connected Flash cells.

A program operation allows to write the 512-byte (x8 device) or 256-word (x16 device) page in typical 200us and an erase operation can be performed in typical 2ms on a 16K-byte (X8 device) block.

Data in the page can be read out at 30ns cycle time (3.3V device) per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, ALE and CLE input pin.

The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.

The modify operations can be locked using the $\overline{WP}$ input pin .

The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.

Even the write-intensive systems can take advantage of the HY27US(08/16)12(1/2)B extended reliability of 100K program/erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The chip is offered with the $\overline{CE}$ don't care function. This option allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

The HY27US(08/16)12(1/2)B is available in 48 - TSOP1 12 x 20 mm package, 48 - USOP1 12 x 17 mm, FBGA 9 x 11 mm.

### 1.1 Product List

| PART NUMBER | ORIZATION | VCC RANGE | PACKAGE |
|---|---|---|---|
| HY27US0812(1/2)B | x8 | 2.7V - 3.6 Volt | 48TSOP1/ 48USOP1/ 63FBGA |
| HY27US1612(1/2)B | x16 | | 48TSOP1 |

**HY27US(08/16)12(1/2)B Series**
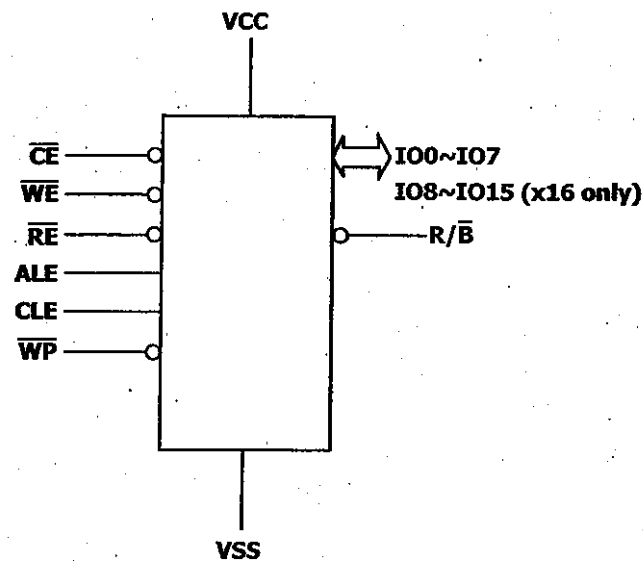**512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**



**Figure1: Logic Diagram**

| IO15 - IO8 | Data Input / Outputs (x16 only) |
|---|---|
| IO7 - IO0 | Data Inputs / Outputs |
| CLE | Command latch enable |
| ALE | Address latch enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{RE}$ | Read Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{WP}$ | Write Protect |
| R/$\overline{B}$ | Ready / Busy |
| Vcc | Power Supply |
| Vss | Ground |
| NC | No Connection |

**Table 1: Signal Names**

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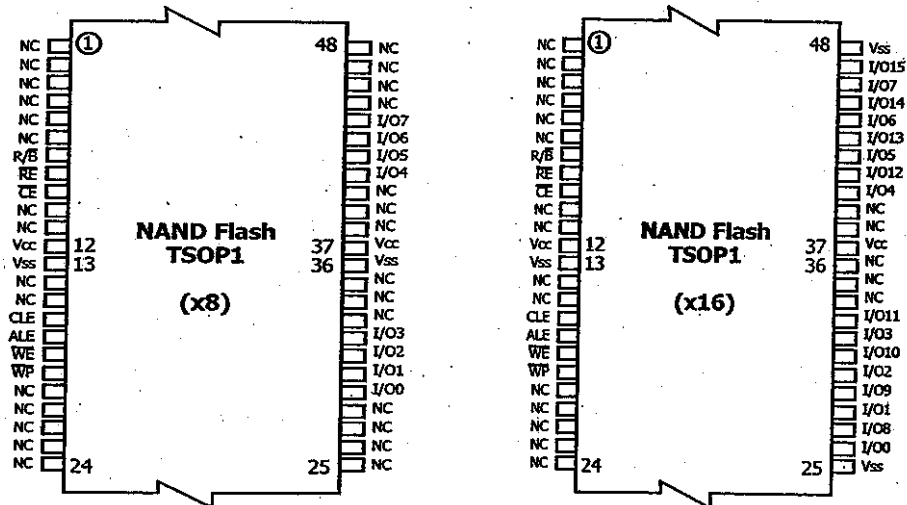
Figure 2. 48TSOP1 Contactions, x8 and x16 Device
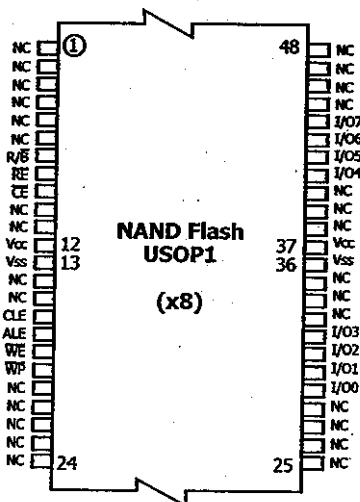


Figure 3. 48USOP1 Contactions, x8

hynix
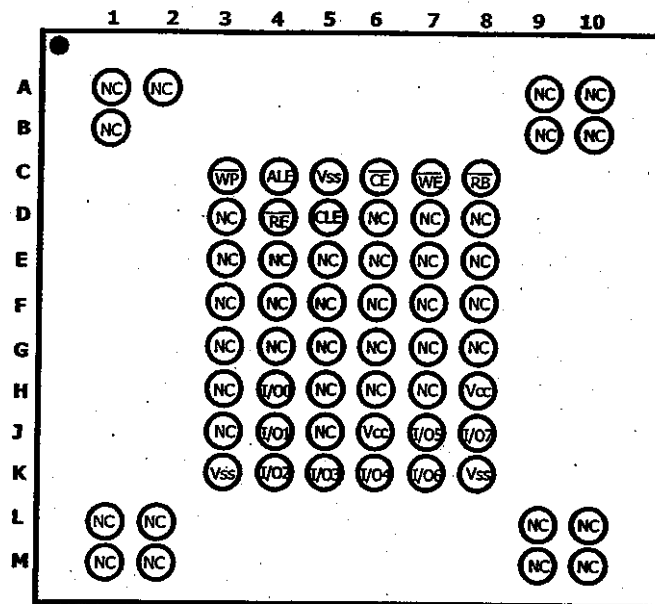
Figure 4. 63FBGA Contactions, x8 Device (Top view through package)

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## 1.2 PIN DESCRIPTION

| Pin Name | Description |
|---|---|
| IO0-IO7 IO8-IO15(1) | **DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (WE). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled. |
| CLE | **COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable (WE). |
| ALE | **ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable (WE). |
| $\overline{CE}$ | **CHIP ENABLE** This input controls the selection of the device. When the device is busy $\overline{CE}$ low does not deselect the memory. |
| $\overline{WE}$ | **WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$. |
| $\overline{RE}$ | **READ ENABLE** The RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one. |
| $\overline{WP}$ | **WRITE PROTECT** The WP pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations. |
| R/$\overline{B}$ | **READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory. |
| VCC | **SUPPLY VOLTAGE** The VCC supplies the power for all the operations (Read, Write, Erase). |
| VSS | GROUND |
| NC | NO CONNECTION |

**Table 2: Pin Description**

**NOTE:**

1. For x16 Version Only
2. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

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|  | IO0 | IO1 | IO2 | IO3 | IO4 | IO5 | IO6 | IO7 |
|---|---|---|---|---|---|---|---|---|
| 1st Cycle | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 |
| 2nd Cycle | A9 | A10 | A11 | A12 | A13 | A14 | A15 | A16 |
| 3rd Cycle | A17 | A18 | A19 | A20 | A21 | A22 | A23 | A24 |
| 4th Cycle | A25 | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ |

Table 3: Address Cycle Map(x8)

**NOTE:**
1. L must be set to Low.
2. A8 is set to LOW or High by the 00h or 01h Command.

|  | IO0 | IO1 | IO2 | IO3 | IO4 | IO5 | IO6 | IO7 | IO8-IO15 |
|---|---|---|---|---|---|---|---|---|---|
| 1st Cycle | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | $L^{(1)}$ |
| 2nd Cycle | A9 | A10 | A11 | A12 | A13 | A14 | A15 | A16 | $L^{(1)}$ |
| 3rd Cycle | A17 | A18 | A19 | A20 | A21 | A22 | A23 | A24 | $L^{(1)}$ |
| 4th Cycle | A25 | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ | $L^{(1)}$ |

Table 4: Address Cycle Map(x16)

**NOTE:**
1. L must be set to Low.

| FUNCTION | 1st CYCLE | 2nd CYCLE | 3rd CYCLE | 4th CYCLE | Acceptable command during busy |
|---|---|---|---|---|---|
| READ 1 | 00h/01h | - | - | - | |
| READ 2 | 50h | - | - | - | |
| READ ID | 90h | - | - | - | |
| RESET | FFh | - | - | - | Yes |
| PAGE PROGRAM (start) | 80h | 10h | - | - | |
| COPY BACK PGM (start) | 00h | 8Ah | - | - | |
| BLOCK ERASE | 60h | D0h | - | - | |
| READ STATUS REGISTER | 70h | - | - | - | Yes |

Table 5: Command Set

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| CLE | ALE | CE̅ | WE̅ | RE̅ | WP̅ | MODE | |
|-----|-----|-----|-----|-----|-----|------|--|
| H | L | L | Rising | H | X | Read Mode | Command Input |
| L | H | L | Rising | H | X | | Address Input(4 cycles) |
| H | L | L | Rising | H | H | Write Mode | Command Input |
| L | H | L | Rising | H | H | | Address Input(4 cycles) |
| L | L | L | Rising | H | H | Data Input | |
| L | L | L(1) | H | Falling | X | Sequential Read and Data Output | |
| L | L | L | H | H | X | During Read (Busy) | |
| X | X | X | X | X | H | During Program (Busy) | |
| X | X | X | X | X | H | During Erase (Busy) | |
| X | X | X | X | X | L | Write Protect | |
| X | X | H | X | X | 0V/Vcc | Stand By | |

**Table 6: Mode Selection**

NOTE:

1. With the CE̅ high during latency time does not stop the read operation

**ʰɣɳɪx**

## 2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

### 2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See figure 6 and table 13 for details of the timings requirements. Command codes are always applied on IO7:0, disregarding the bus configuration (X8/X16).

### 2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. To insert the 25 addresses needed to access the 512Mbit 4 clock cycles (x8 version) are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See figure 7 and table 13 for details of the timings requirements. Addresses are always applied on IO7:0, disregarding the bus configuration (X8/X16).

### 2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See figure 8 and table 13 for details of the timings requirements.

### 2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See figures 9 to 15 and table 13 for details of the timings requirements.

### 2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

### 2.6 Standby.

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced.

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## 3. DEVICE OPERATION

### 3.1 Page Read.

Three types of operations are available: random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes (x8 device) or 264 words (x16 device) of data within the selected page are transferred to the data registers in less than access random read time tR (12us). The system controller can detect the completion of this data transfer tR (12us) by analyzing the output of R/B̄ pin. Once the data in a page is loaded into the registers, they may be read out in 30ns cycle time by sequentially pulsing RĒ. High to low transitions of the RĒ clock output the data stating from the selected column address up to the last column address.

After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting tR again allows reading the selected page. The sequential row read operation is terminated by bringing CĒ high.

The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. Writing the Read2 command user may selectively access the spare area of bytes 512 to 527 (x8 device) or words 256 to 263 (x16 device). Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row

Read as in Read1 operation and spare sixteen bytes of each page (x8 device) or eight words of each page (x16 device) may be sequentially read. The Read1 command (00h/01h) is needed to move the pointer back to the main area. The Read2 command (50h) is needed to move the pointer back to the spare area.

Figure_11 to 14 show typical sequence and timings for each read operation.

### 3.2 Page Program.

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528 (x8 device), in a single page program cycle. The number of consecutive partial page programming operations within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes (x8 device) or 264 word (x16 device) of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to Figure 24 The data-loading sequence begins by inputting the Serial Data Input command (80h), followed by the four address input cycles and then serial data loading. The Page Program confirm command (10h) starts the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal Program Erase Controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with RĒ and CĒ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B̄ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked in Figure 15 The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

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## 3.3 Block Erase.

The Erase operation is done on a block (16K Byte) basis. It consists of an Erase Setup command (60h), a Block address loading and an Erase Confirm Command (D0h). The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

The block address loading is accomplished three cycles. Only block addresses (A14 to A25 , highest address depending on the device density) are needed while A9 to A13 is ignored.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal Program Erase Controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. Figure 17 details the sequence.

## 3.4 Copy-Back Program.

The copy-back program is provided to quickly and efficiently rewrite data stored in one page within the plane to another page within the same plane without using an external memory. Since the time-consuming sequential reading and its reloading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without burst-reading cycle and copying-program with the address of destination page. A normal read operation with "00h" command and the address of the source page moves the whole 528byte data into the internal buffer.

As soon as the device returns to Ready state, Page-Copy Data-input command (8Ah) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is not needed to actually begin the programming operation. For backward-compatibility, issuing Program Confirm command during copy-back does not affect correct device operation.

Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. Plane address must be the same between source and target page.

"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."

Figure 16 shows the command sequence for the copy-back operation.

**The Copy Back Program operation requires three steps:**

1. The source page must be read using the Read A command (one bus write cycle to setup the command and then 4 bus write cycles to input the source page address). This operation copies all 2KBytes from the page into the Page Buffer.

2. When the device returns to the ready state (Ready/Busy High), the second bus write cycle of the command is given with the 4bus cycles to input the target page address. The value for A25 from second to the last page address must be same as the value given to A25 in first address.

3. Then the confirm command is issued to start the P/E/R Controller.

**hynix**

## 3.5 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operatio is completed, and whether the read, program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two-line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 14 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h or 50h) should be given before sequential page read cycle.

## 3.6 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the 1st cycle (ADh), and 2nd cycle (the device code) and 3rd cycle ID, 4th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 18 shows the operation sequence, while Tables 16 explain the byte meaning.

## 3.7 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased.

The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 14 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 21 below.

**hynix**

## 4. OTHER FEATURES

### 4.1 Data Protection for Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.0V(3.0V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 22. The two-step command sequence for program/erase provides additional software protection.

### 4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied.

Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart in Figure 23. Its value can be determined by the following guidance.

**hynix**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Valid Block Number | N$_{VB}$ | 4016 | | 4096 | Blocks |

**Table 7: Valid Blocks Number**

**NOTE:**

1. The 1st block is guaranteed to be a valid block up to 1K cycles with ECC. (1bit/528bytes)

| Symbol | Parameter | Value 3.3V | Unit |
|---|---|---|---|
| T$_A$ | Ambient Operating Temperature (Temperature Range Option 1) | 0 to 70 | ℃ |
| | Ambient Operating Temperature (Industrial Temperature Range) | -40 to 85 | ℃ |
| T$_{BIAS}$ | Temperature Under Bias | -50 to 125 | ℃ |
| T$_{STG}$ | Storage Temperature | -65 to 150 | V |
| V$_{IO}$(2) | Input or Output Voltage | -0.6 to 4.6 | V |
| V$_{CC}$ | Supply Voltage | -0.6 to 4.6 | V |

**Table 8: Absolute maximum ratings**

**NOTE:**

1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute
   Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of
   the device at these or any other conditions above those indicated in the Operating sections of this specification is
   not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

**hynix**
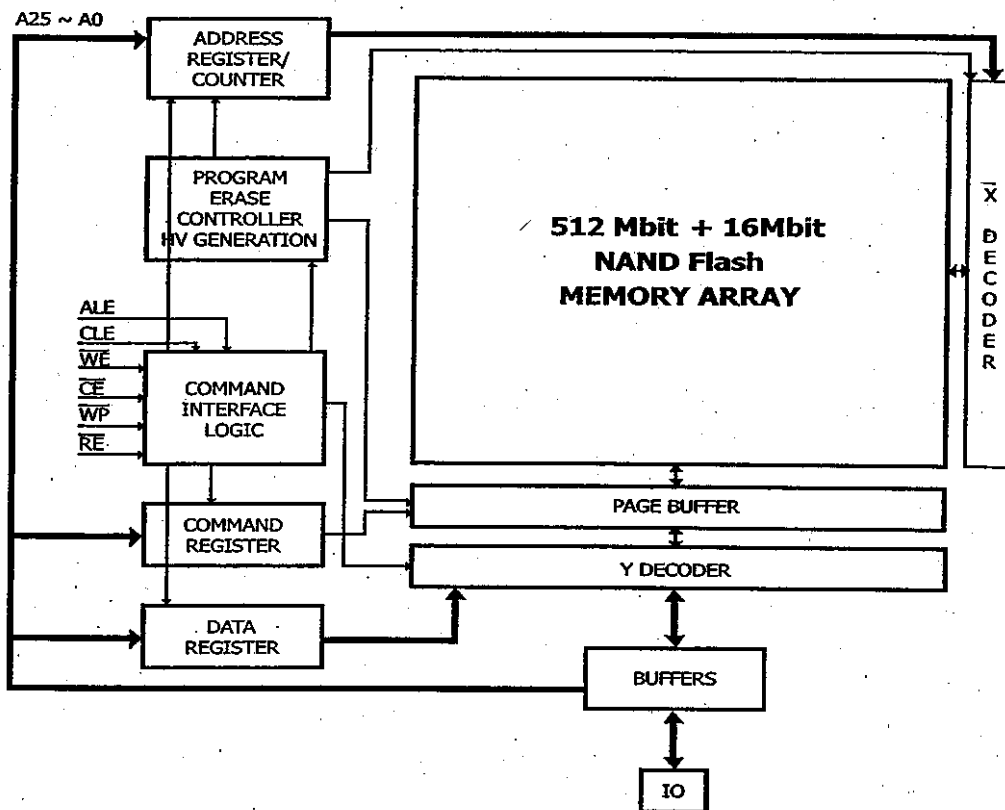
Figure 5: Block Diagram

**hynix**

| Parameter | | Symbol | Test Conditions | 3.3Volt | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Operating Current | Sequential Read | $I_{CC1}$ | $t_{RC}$=30ns, $\overline{CE}$=$V_{IL}$, $I_{OUT}$=0mA | - | 15 | 30 | mA |
| | Program | $I_{CC2}$ | - | - | 15 | 30 | mA |
| | Erase | $I_{CC3}$ | - | - | 15 | 30 | mA |
| Stand-by Current (TTL) | | $I_{CC4}$ | $\overline{CE}$=$V_{IH}$, $\overline{WP}$=0V/Vcc | - | - | 1 | mA |
| Stand-by Current (CMOS) | | $I_{CC5}$ | $\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc | - | 10 | 50 | uA |
| Input Leakage Current | | $I_{LI}$ | $V_{IN}$=0 to Vcc (max) | - | - | ± 10 | uA |
| Output Leakage Current | | $I_{LO}$ | $V_{OUT}$ =0 to Vcc (max) | - | - | ± 10 | uA |
| Input High Voltage | | $V_{IH}$ | - | Vccx0.8 | - | Vcc+0.3 | V |
| Input Low Voltage | | $V_{IL}$ | - | -0.3 | - | Vccx0.2 | V |
| Output High Voltage Level | | $V_{OH}$ | $I_{OH}$=-400uA | 2.4 | - | - | V |
| Output Low Voltage Leve | | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.4 | V |
| Output Low Current (R/$\overline{B}$) | | $I_{OL}$ (R/$\overline{B}$) | $V_{OL}$=0.4V | 8 | 10 | - | mA |

**Table 9: DC and Operating Characteristics**

| Parameter | Value |
|---|---|
| | 3.3Volt |
| Input Pulse Levels | 0V to Vcc |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | Vcc / 2 |
| Output Load (2.7V - 3.6V) | 1 TTL GATE and CL=50pF |

**Table 10: AC Conditions**

# hynix

| Item | Symbol | Test Condition | Min | Max | Unit |
|------|--------|----------------|-----|-----|------|
| Input / Output Capacitance | $C_{I/O}$ | $V_{IL}=0V$ | - | 10 | pF |
| Input Capacitance | $C_{IN}$ | $V_{IN}=0V$ | - | 10 | pF |

**Table 11: Pin Capacitance (TA=25C, F=1.0MHz)**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|-----------|--|--------|-----|-----|-----|------|
| Program Time | | $t_{PROG}$ | - | 200 | 700 | us |
| Number of partial Program Cycles in the same page | Main Array | NOP | - | - | 1 | Cycles |
| | Spare Array | NOP | - | - | 2 | Cycles |
| Block Erase Time | | $t_{BERS}$ | - | 2 | 3 | ms |

**Table 12: Program / Erase Characteristics**

**hynix**

HY27US(08/16)12(1/2)B Series
512Mbit (64Mx8bit / 32Mx16bit) NAND Flash

| Parameter | Symbol | 3.3Volt | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| CLE Setup time | tCLS | 15 | | ns |
| CLE Hold time | tCLH | 5 | | ns |
| $\overline{CE}$ setup time | tCS | 20 | | ns |
| $\overline{CE}$ hold time | tCH | 5 | | ns |
| $\overline{WE}$ pulse width | tWP | 15 | | ns |
| ALE setup time | tALS | 15 | | ns |
| ALE hold time | tALH | 5 | | ns |
| Data setup time | tDS | 15 | | ns |
| Data hold time | tDH | 5 | | ns |
| Write Cycle time | tWC | 30 | | ns |
| $\overline{WE}$ High hold time | tWH | 10 | | ns |
| Data Transfer from Cell to register | tR | | 12 | us |
| ALE to $\overline{RE}$ Delay | tAR | 10 | | ns |
| CLE to $\overline{RE}$ Delay | tCLR | 10 | | ns |
| Ready to $\overline{RE}$ Low | tRR | 20 | | ns |
| $\overline{RE}$ Pulse Width | tRP | 15 | | ns |
| $\overline{WE}$ High to Busy | tWB | | 100 | ns |
| Read Cycle Time | tRC | 30 | | ns |
| $\overline{RE}$ Access Time | tREA | | 18 | ns |
| $\overline{RE}$ High to Output High Z | tRHZ | | 50 | ns |
| $\overline{CE}$ High to Output High Z | tCHZ | | 50 | ns |
| $\overline{RE}$ or $\overline{CE}$ high to Output hold | tOH | 10 | | ns |
| $\overline{RE}$ High Hold Time | tREH | 10 | | ns |
| Output High Z to $\overline{RE}$ low | tIR | 0 | | ns |
| $\overline{CE}$ Access Time | tCEA | | 25 | ns |
| $\overline{WE}$ High to $\overline{RE}$ low | tWHR | 60 | | ns |
| Last $\overline{RE}$ High to busy (at sequential read) | tRB | | 100 | ns |
| $\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at read) | tCRY | | 60+tr(R/B#)[4] | ns |
| $\overline{CE}$ High Hold Time (at the last serial read)[3] | tCEH | 100 | | ns |
| Device Resetting Time (Read / Program / Erase) | tRST | | 5/10/500[1,2] | us |
| Write Protection time | tWW[5] | 100 | | ns |

**Table 13: AC Timing Characteristics**

**NOTE:**

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
2. The time to Ready depends on the value of the pull-up resistor tied R/B pin.ting time.
3. To break the sequential read cycle, $\overline{CE}$ must be held for longer time than tCEH.
4. The time to Ready depends on the value of the pull-up resistor tied R/B pin.
5. Program / Erase Enable Operation : $\overline{WP}$ high to $\overline{WE}$ High.
   Program / Erase Disable Operation : $\overline{WP}$ Low to $\overline{WE}$ High.

**hynix**

| IO | Pagae Program | Block Erase | Read | Cache Read | CODING |
|---|---|---|---|---|---|
| 0 | Pass / Fail | Pass / Fail | NA | | Pass: '0' Fail: '1' |
| 1 | NA | NA | NA | | Pass: '0' Fail: '1' (Only for Cache Program, else Don't care) |
| 2 | NA | NA | NA | | - |
| 3 | NA | NA | NA | | - |
| 4 | NA | NA | NA | | - |
| 5 | Ready/Busy | Ready/Busy | Ready/Busy | P/E/R Controller Bit | Active: '0' Idle: '1' |
| 6 | Ready/Busy | Ready/Busy | Ready/Busy | Ready/Busy | Busy: '0' Ready': '1' |
| 7 | Write Protect | Write Protect | Write Protect | | Protected: '0' Not Protected: '1' |

**Table 14: Status Register Coding**

| DEVIIDENTIFIER CYCLE | DESCRIPTION |
|---|---|
| 1st | Manufacturer Code |
| 2nd | Device Identifier |

**Table 15: Device Identifier Coding**

| Part Number | Voltage | Bus Width | 1st cycle (Manufacture Code) | 2nd cycle (Device Code) |
|---|---|---|---|---|
| HY27US0812(1/2)B | 3.3V | x8 | ADh | 76h |
| HY27US1612(1/2)B | 3.3V | x16 | ADh | 56h |

**Table 16: Read ID Data Table**

**hynix**
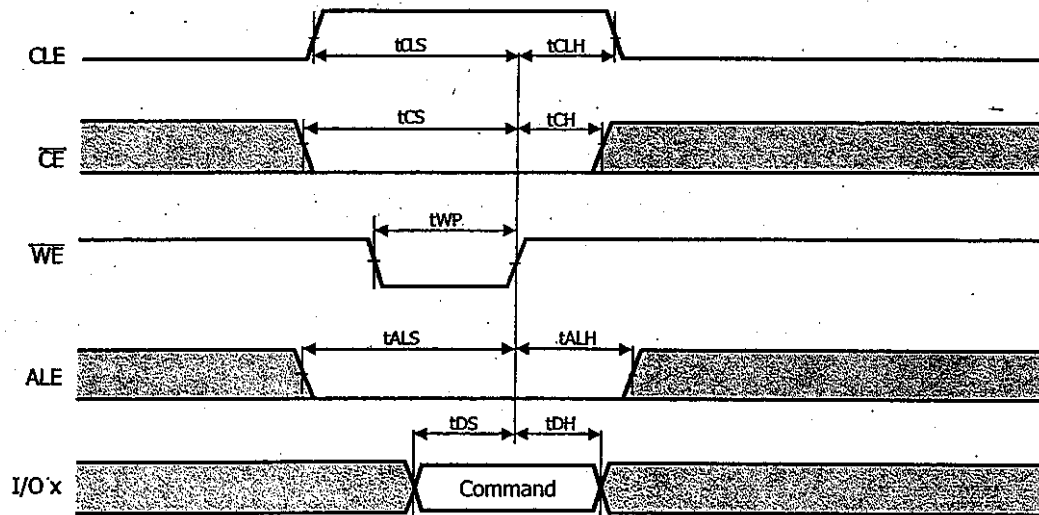
**Figure 6: Command Latch Cycle**
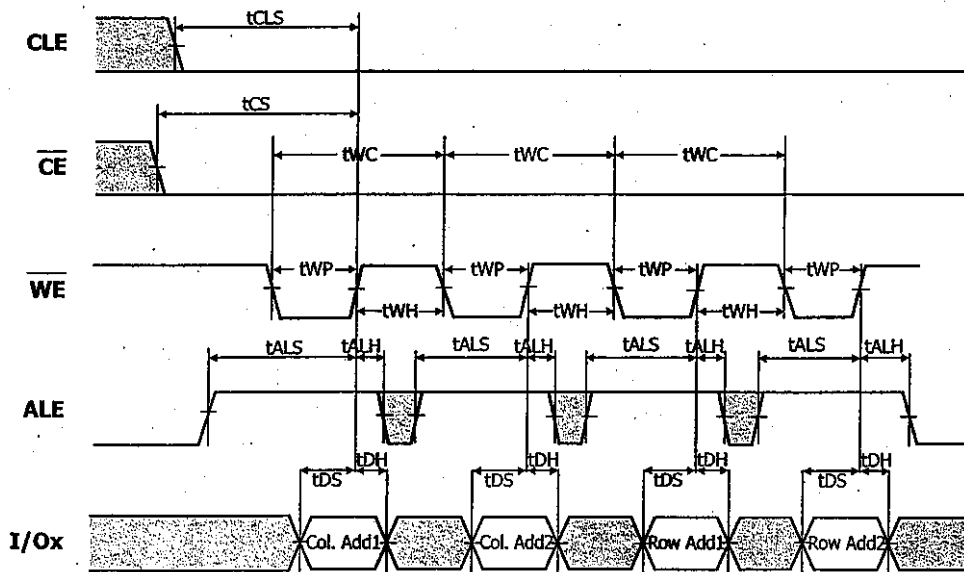


**Figure 7: Address Latch Cycle**

**hynix**



**Figure 8. Input Data Latch Cycle**



Notes : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

**Figure 9: Sequential Out Cycle after Read (CLE=L, WE=H, ALE=L)**
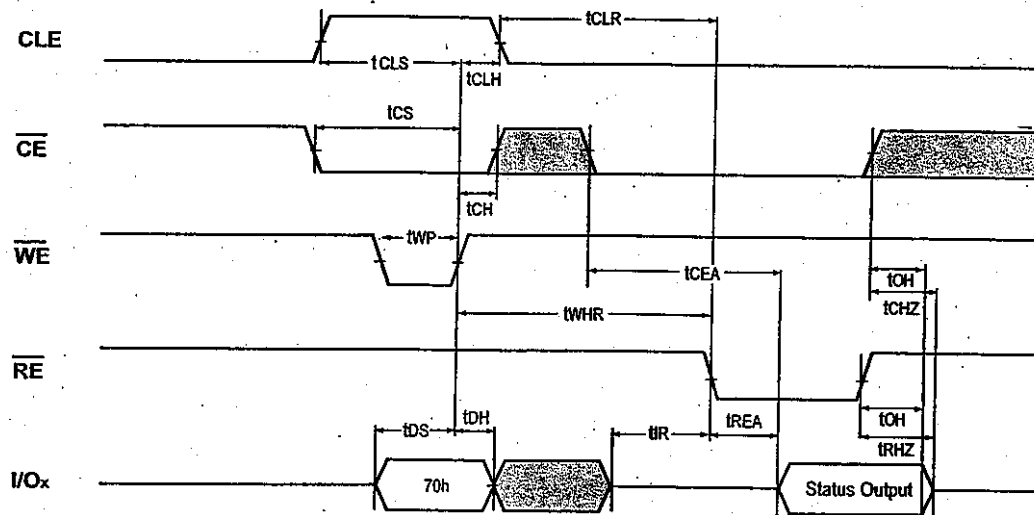
**Figure 10: Status Read Cycle**
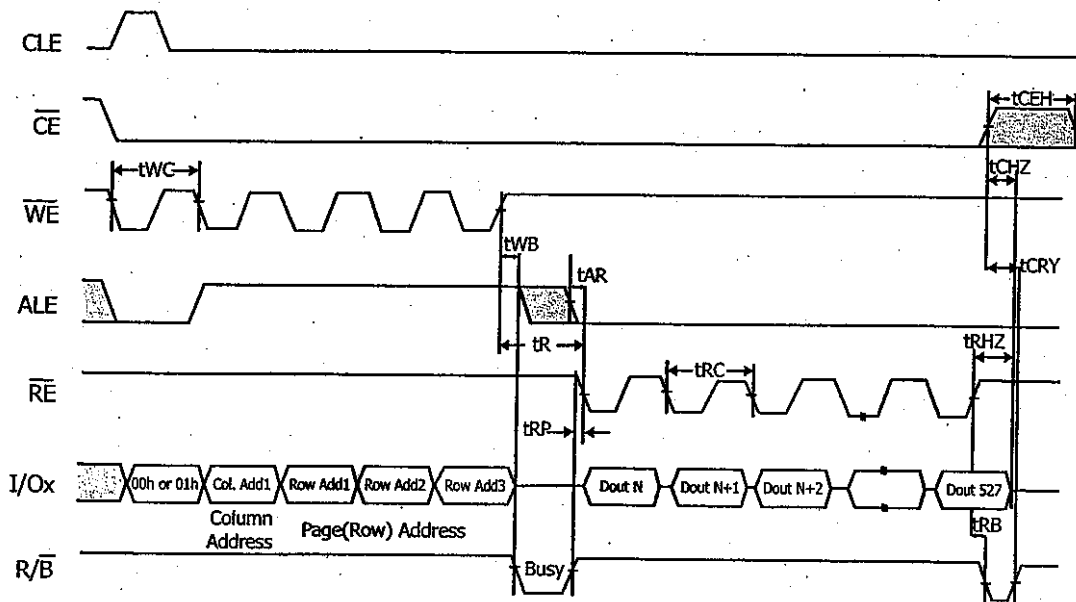


**Figure 11: Read1 Operation (Read One Page)**

**hynix**
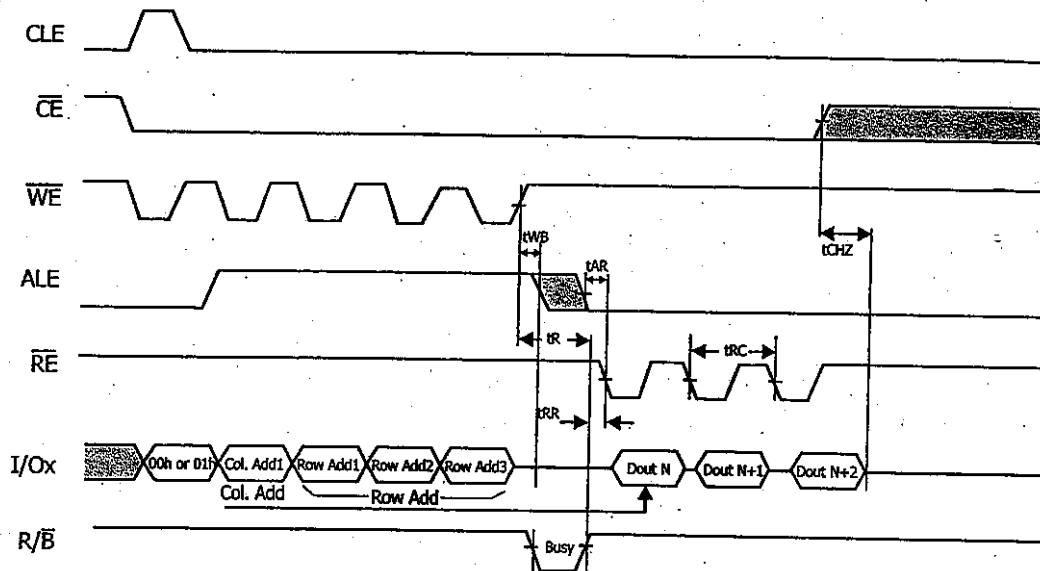
**Figure 12: Read1 Operation intercepted by $\overline{CE}$**
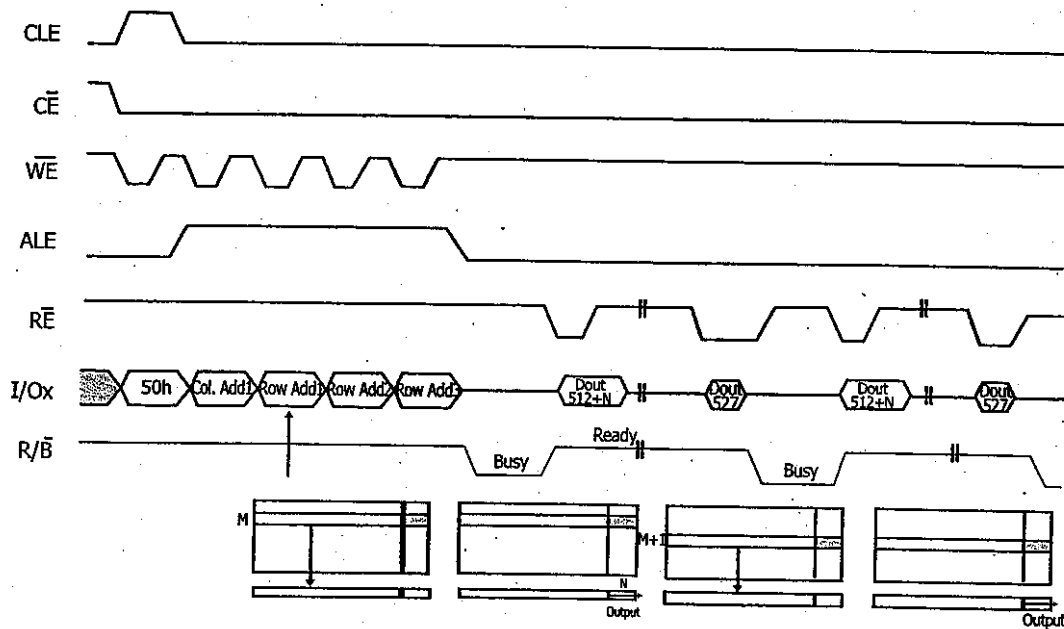


**Figure 13: Read2 Operation (Sequential Row Read)**

hynix
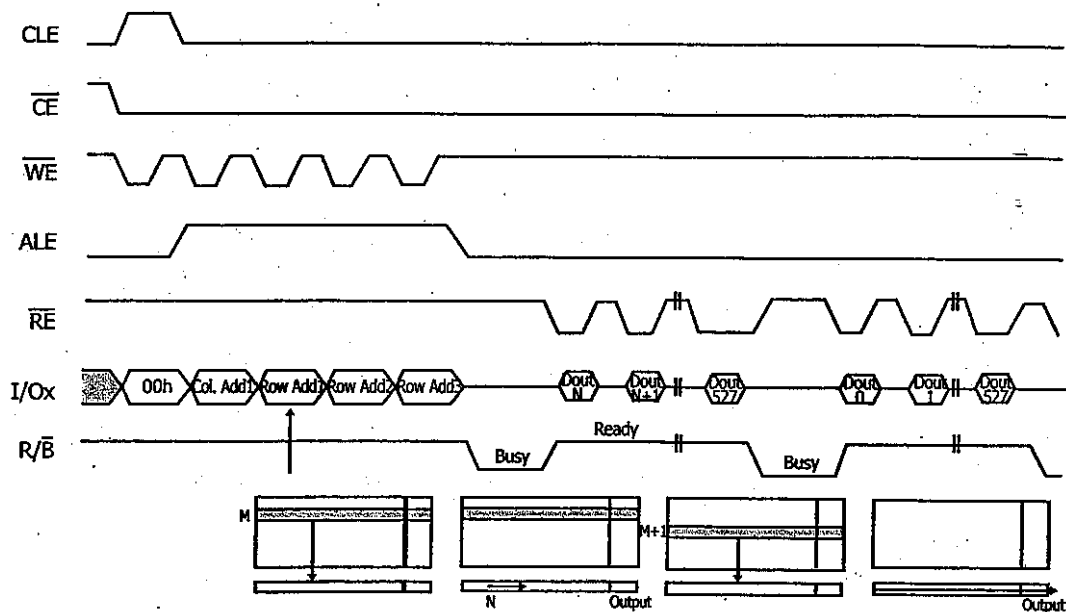


**Figure 14: Sequential Row Read Operation Within a Block**
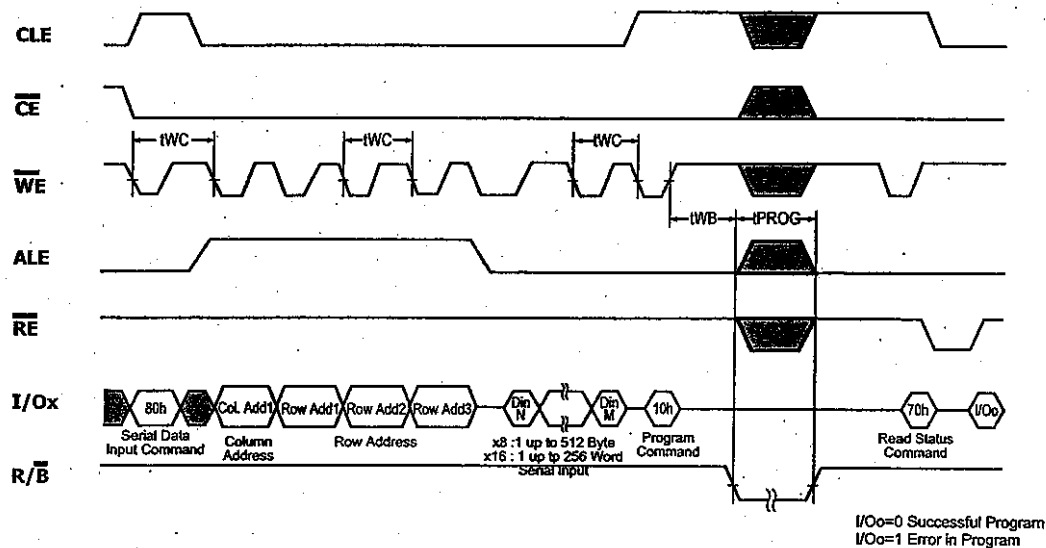


**Figure 15: Page Program Operation**

hynix
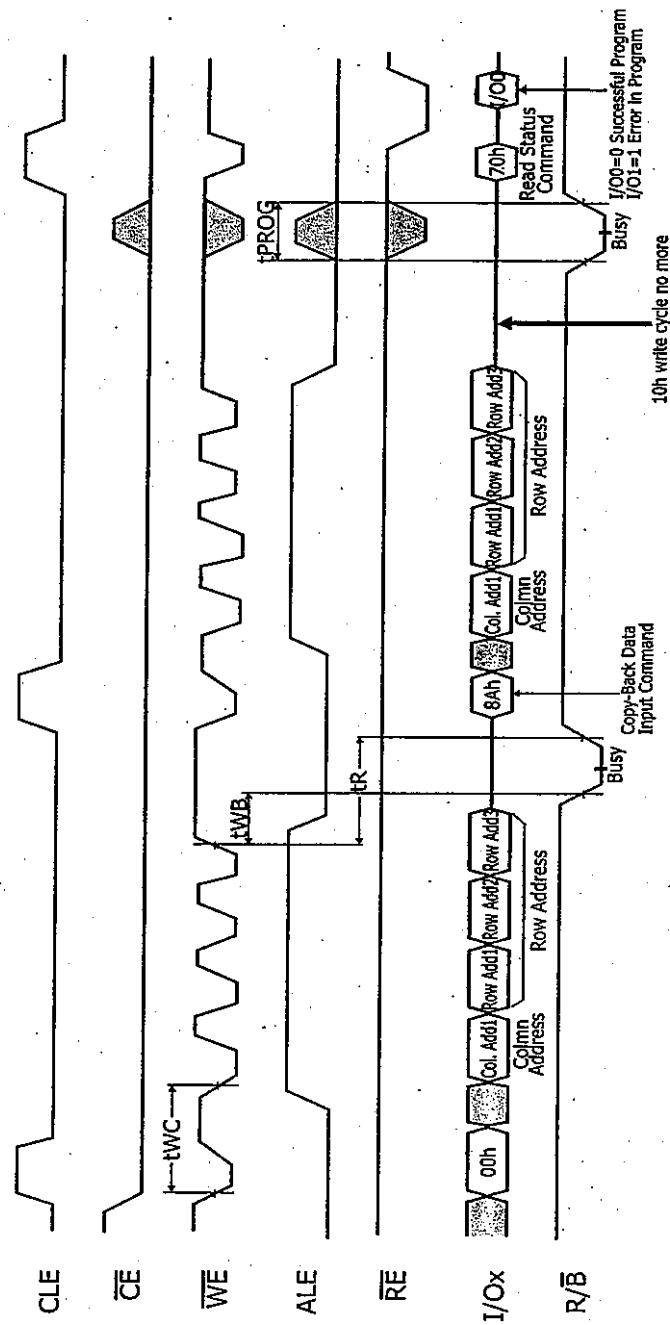


Figure 16 : Copy Back Program

**HY27US(08/16)12(1/2)B Series**
**512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**
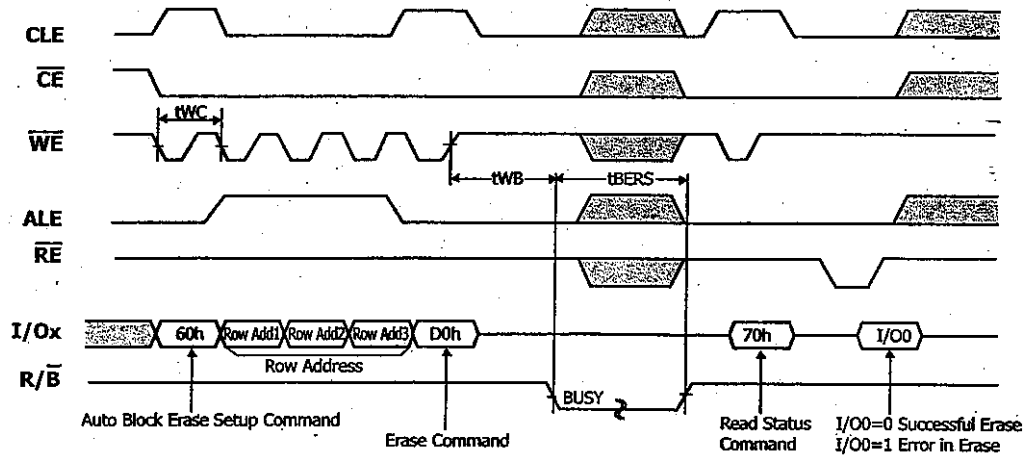


**Figure 17: Block Erase Operation (Erase One Block)**
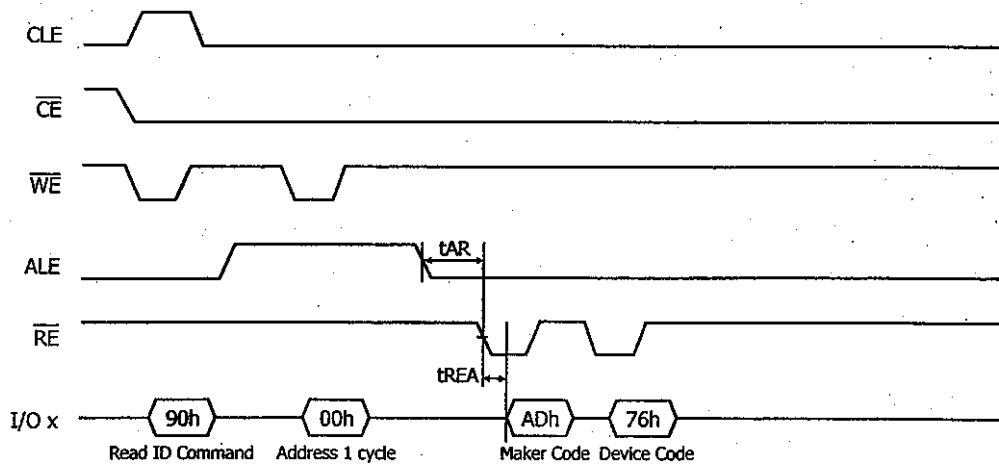


**Figure 18: Read ID Operation**

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**HY27US(08/16)12(1/2)B Series**
**512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**

**System Interface Using CE don't care**
To simplify system interface, CE may be deasserted during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microporcessor. The only function that was removed from standard NAND Flash to make CE don't care read operation was disabling of the automatic sequential read function. (HY27US(08/16)122B)
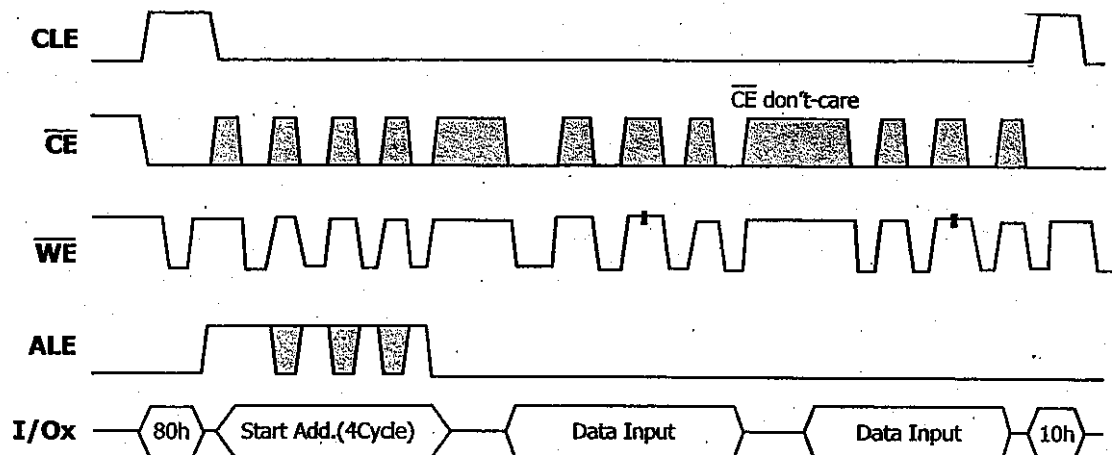
**Figure 19: Program Operation with CE don't-care.**
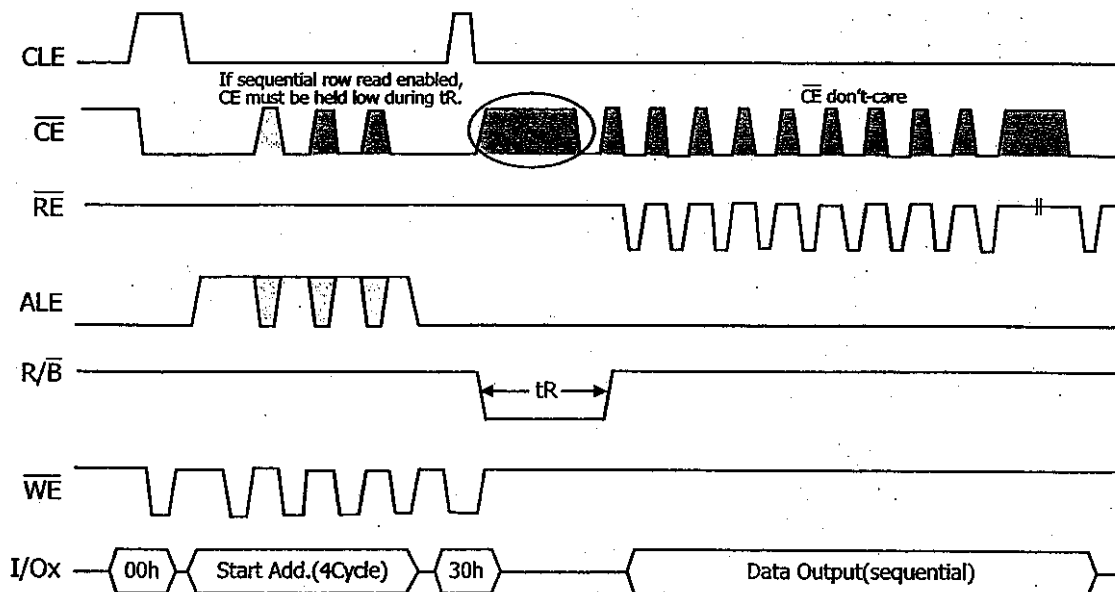
**Figure 20: Read Operation with CE don't-care.**
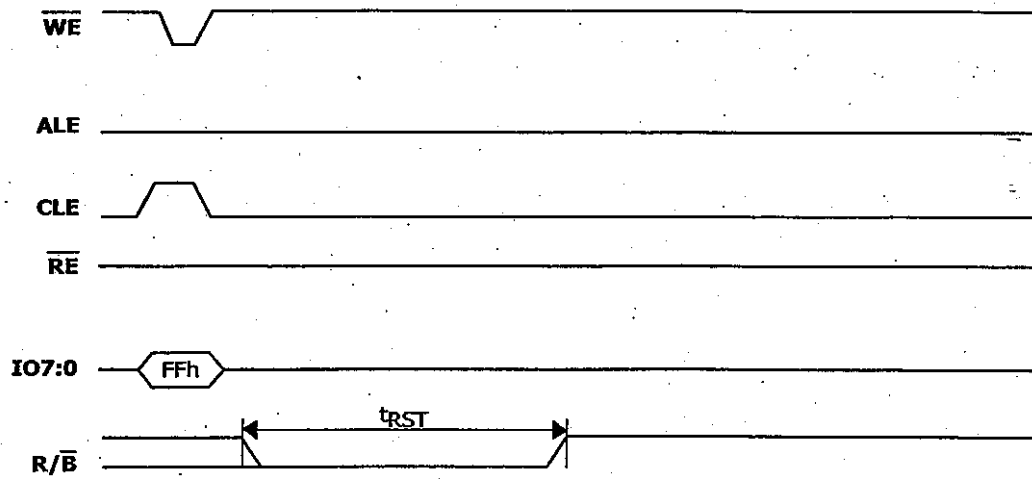
**Figure 21: Reset Operation**
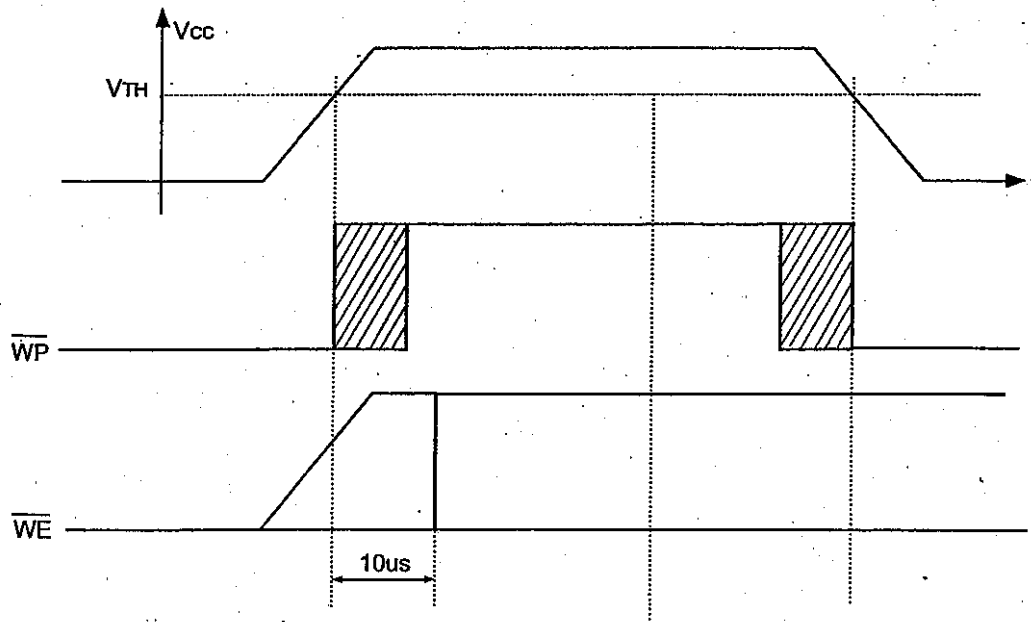


**Figure 22: Power On and Data Protection Timing**

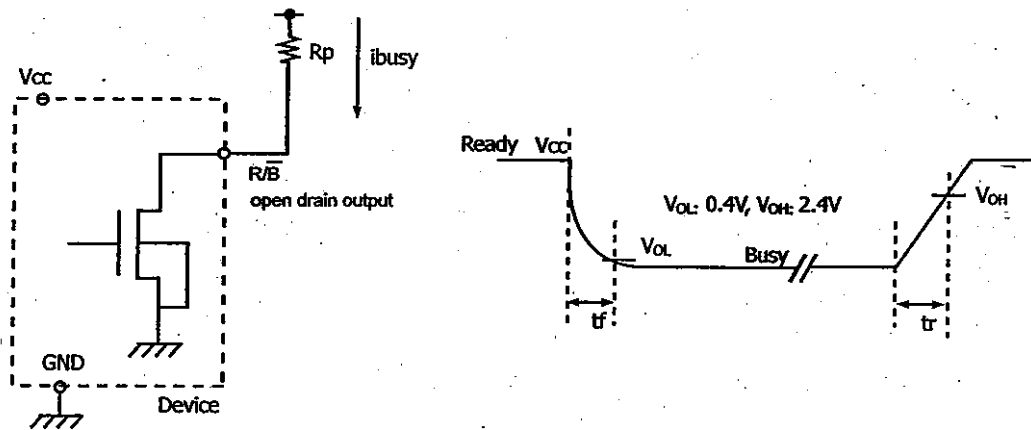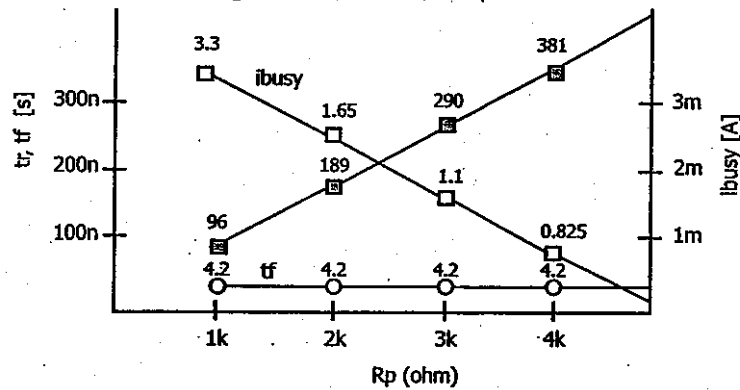**VTH = 2.5 Volt for 3.3 Volt Supply devices**

**hynix**



Fig. Rp vs tr, tf & Rp vs ibusy
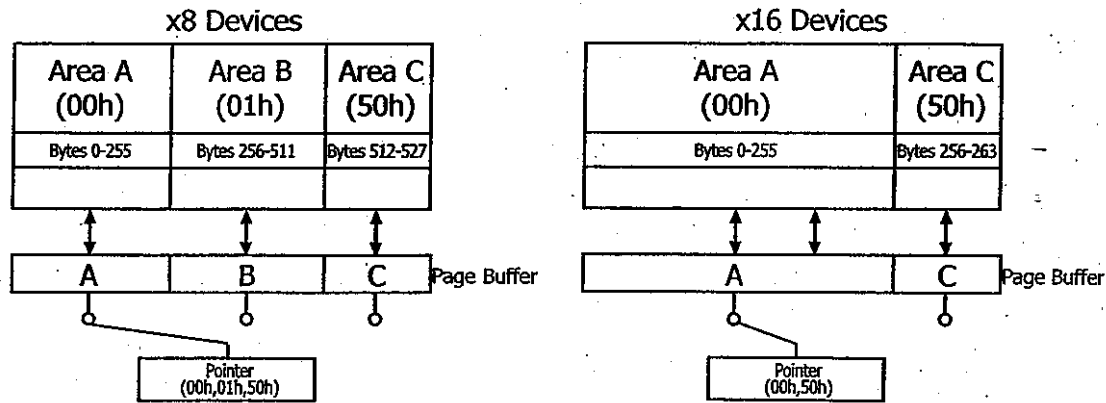
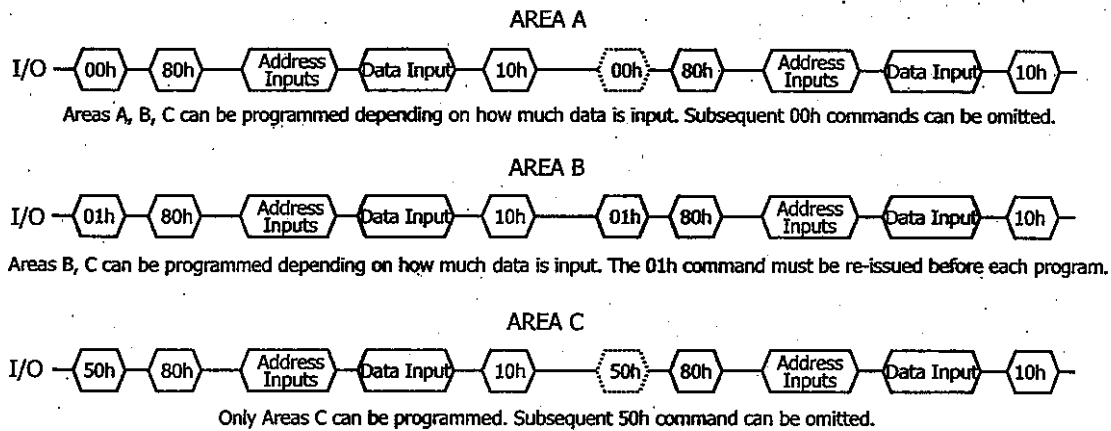@ Vcc = 3.3V, Ta = 25°C, C$_L$=50pF



Rp value guidence

$$Rp\,(min) = \frac{Vcc\,(Max.) - V_{OL}\,(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I$_L$ is the sum of the input currnts of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

**Figure 23: Ready/Busy Pin electrical specifications**

**hynix**

**Figure 24: Pointer operations**



**AREA A**

Areas A, B, C can be programmed depending on how much data is input. Subsequent 00h commands can be omitted.

**AREA B**

Areas B, C can be programmed depending on how much data is input. The 01h command must be re-issued before each program.

**AREA C**

Only Areas C can be programmed. Subsequent 50h command can be omitted.

**Figure 25: Pointer Operations for porgramming**

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**Bad Block Management**

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh).

The Bad Block Information is written prior to shipping. Any block where the 6th Byte/ 3rd Word in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 26. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

**Block Replacement**

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

The Copy Back Program command can be used to copy the data to a valid block.

See the "Copy Back Program" section for more details.

Refer to Table 18 for the recommended procedure to follow if an error occurs during an operation.

| Operation | Recommended Procedure |
|-----------|----------------------|
| Erase | Block Replacement |
| Program | Block Replacement |
| Read | ECC (with 1bit/528byte) |

**Table 18: Block Failure**
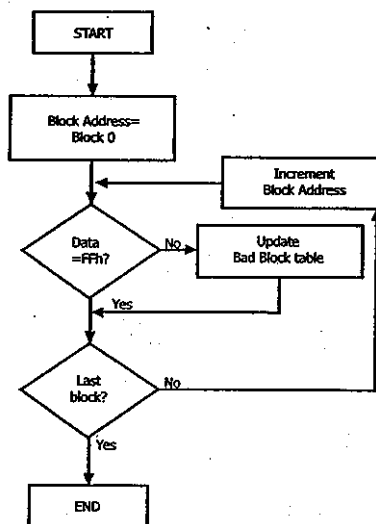


**Figure 26: Bad Block Management Flowchart**

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## Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 27~30)



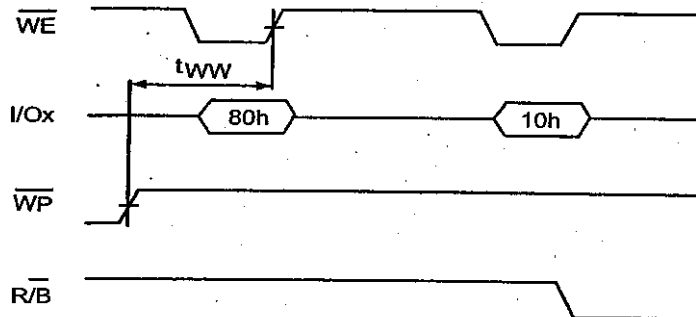Figure 27: Enable Programming



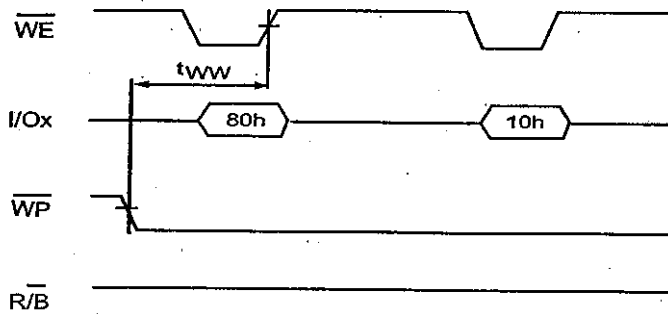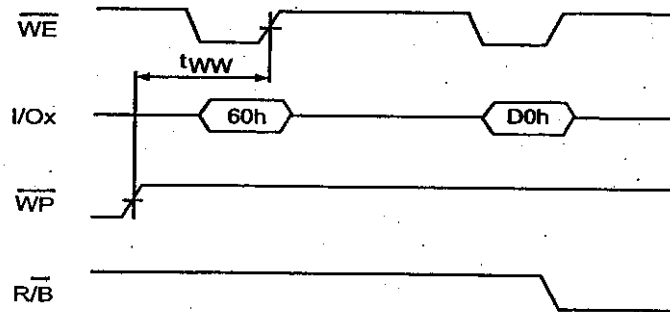Figure 28: Disable Programming

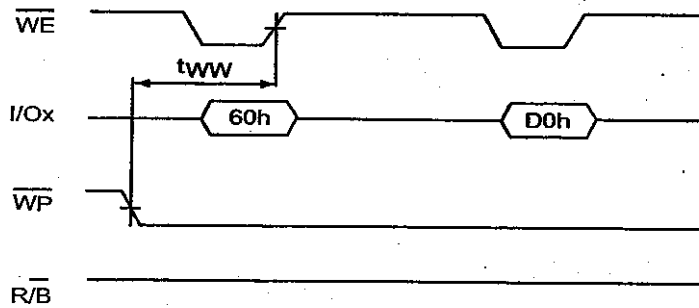# hynix

**Figure 29: Enable Erasing**

**Figure 30: Disable Erasing**

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HY27US(08/16)12(1/2)B Series
512Mbit (64Mx8bit / 32Mx16bit) NAND Flash
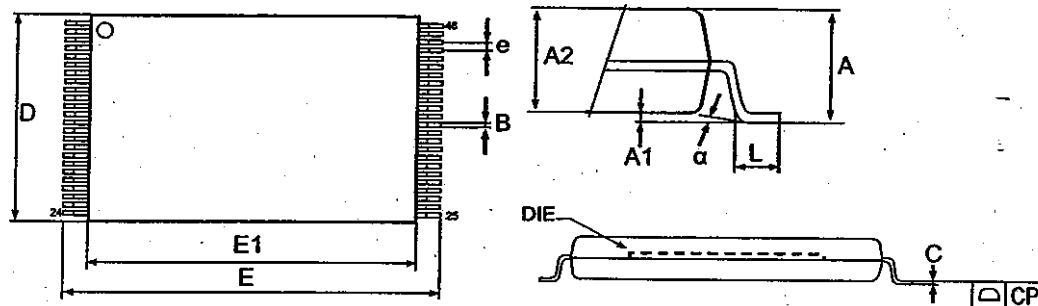


Figure 31: 48pin-TSOP1, 12 x 20mm, Package Outline

| Symbol | millimeters | | |
|--------|-------------|--------|--------|
|        | Min | Typ | Max |
| A      |     |     | 1.200 |
| A1     | 0.050 |   | 0.150 |
| A2     | 0.980 |   | 1.030 |
| B      | 0.170 |   | 0.250 |
| C      | 0.100 |   | 0.200 |
| CP     |     |     | 0.100 |
| D      | 11.910 | 12.000 | 12.120 |
| E      | 19.900 | 20.000 | 20.100 |
| E1     | 18.300 | 18.400 | 18.500 |
| e      |     | 0.500 |     |
| L      | 0.500 |   | 0.680 |
| alpha  | 0   |     | 5 |

Table 19: 48pin-TSOP1, 12 x 20mm, Package Mechanical Data

**hynix**

**HY27US(08/16)12(1/2)B Series
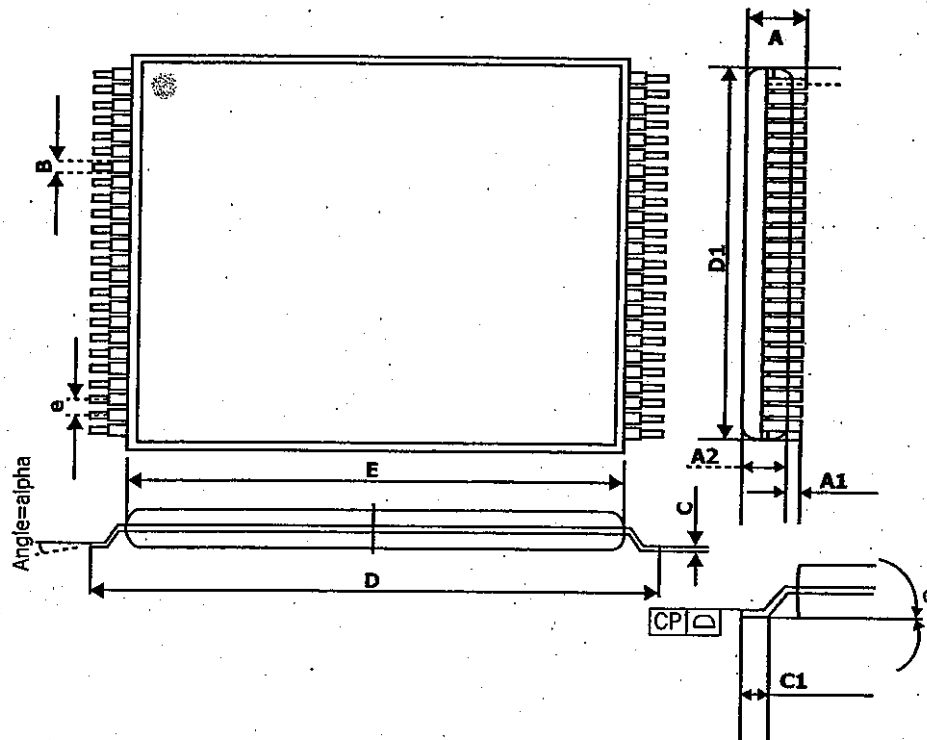512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**



**Figure 32. 48pin-USOP1, 12 x 17mm, Package Outline**

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | | | 0.650 |
| A1 | 0 | 0.050 | 0.080 |
| A2 | 0.470 | 0.520 | 0.570 |
| B | 0.130 | 0.160 | 0.230 |
| C | 0.065 | 0.100 | 0.175 |
| C1 | 0.450 | 0.650 | 0.750 |
| CP | | | 0.100 |
| D | 16.900 | 17.000 | 17.100 |
| D1 | 11.910 | 12.000 | 12.120 |
| E | 15.300 | 15.400 | 15.500 |
| e | | 0.500 | |
| alpha | 0 | | 8 |

**Table 20: 48pin-USOP1, 12 x 17mm, Package Mechanical Data**

**hynix**

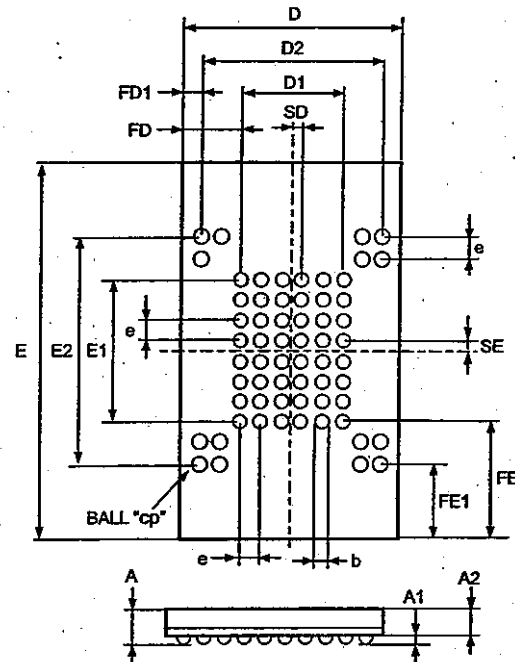**HY27US(08/16)12(1/2)B Series**
**512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**



**Figure 33. 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Pakage Outline**

NOTE: Drawing is not to scale.

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.25 | 0.30 | 0.35 |
| A2 | 0.55 | 0.60 | 0.65 |
| b | 0.40 | 0.45 | 0.50 |
| D | 8.90 | 9.00 | 9.10 |
| D1 | | 4.00 | |
| D2 | | 7.20 | |
| E | 10.90 | 11.00 | 11.10 |
| E1 | | 5.60 | |
| E2 | | 8.80 | |
| e | | 0.80 | |
| FD | | 2.50 | |
| FD1 | | 0.90 | |
| FE | | 2.70 | |
| FE1 | | 1.10 | |
| SD | | 0.40 | |
| SE | | 0.40 | |

# hynix

**HY27US(08/16)12(1/2)B Series**
**512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**

## MARKING INFORMATION - TSOP1/USOP

| Packag | Marking Example |
|---|---|

| TSOP1 / USOP | hynix    K O R<br>H Y 2 7 U S x x 1 2 x B<br>x x x x    Y W W x x |
|---|---|

| - hynix | : Hynix Symbol |
|---|---|
| - KOR | : Origin Country |

| - HY27USxx12xB xxxx | : Part Number |
|---|---|
| **HY:** Hynix | |
| **27:** NAND Flash | |
| **U:** Power Supply | : U(2.7V~3.6V) |
| **S:** Classification | : Single Level Cell+Single Die+Small Block |
| **xx:** Bit Organization | : 08(x8), 16(x16) |
| **12:** Density | : 512Mbit |
| **x:** Mode | : 1nCE & 1R/nB; Sequential Row Read Enable |
| | : 1nCE & 1R/nB; Sequential Row Read Disable |
| **B:** Version | : 3rd Generation |
| **x:** Package Type | : T(48-TSOP1), S(48-USOP) |
| **x:** Package Material | : Blank(Normal), P(Lead Free) |
| **x:** Operating Temperature | : C(0℃~70℃), I(-40℃~85℃) |
| **x:** Bad Block | : B(Included Bad Block), S(1~5 Bad Block), P(All Good Block) |
| - **Y:** Year (ex: 5=year 2005, 06= year 2006) | |
| - **ww:** Work Week (ex: 12= work week 12) | |
| - **xx:** Process Code | |

| **Note** | |
|---|---|
| - Capital Letter | : Fixed Item |
| - Small Letter | : Non-fixed Item |

# hynix

**HY27US(08/16)12(1/2)B Series**
**512Mbit (64Mx8bit / 32Mx16bit) NAND Flash**

## MARKING INFORMATION - FBGA

| Packag | Marking Example |
|---|---|
| FBGA | hynix  [K][O][R]  [H][Y][2][7][U][S][0][8][1][2][x][B]  [x][x][x][x]    [Y][W][W][x][x] |

|  |  |
|---|---|
| - hynix | : Hynix Symbol |
| - KOR | : Origin Country |
| - HY27U0812xB xxxx | : Part Number |
| HY: Hynix | |
| 27: NAND Flash | |
| U: Power Supply | : U(2.7V~3.6V) |
| S: Classification | : Single Level Cell+Single Die+Small Block |
| 08: Bit Organization | : 08(x8) |
| 12: Density | : 512Mbit |
| x: Mode | : 1nCE & 1R/nB; Sequential Row Read Enable |
| | : 1nCE & 1R/nB; Sequential Row Read Disable |
| B: Version | : 3rd Generation |
| x: Package Type | : F(63FBGA) |
| x: Package Material | : Blank(Normal), P(Lead Free) |
| x: Operating Temperature | : C(0℃~70℃), I(-40℃~85℃) |
| x: Bad Block | : B(Included Bad Block), S(1~5 Bad Block), P(All Good Block) |
| - Y: Year (ex: 5=year 2005, 06= year 2006) | |
| - ww: Work Week (ex: 12= work week 12) | |
| - xx: Process Code | |
| **Note** | |
| - Capital Letter | : Fixed Item |
| - Small Letter | : Non-fixed Item |

# EXHIBIT 3
## TO LAI DECLARATION

# HIGHLY CONFIDENTIAL – ATTORNEYS EYES ONLY

# EXHIBIT FILED UNDER SEAL

# EXHIBIT 4
## TO LAI DECLARATION

# HIGHLY CONFIDENTIAL – ATTORNEYS EYES ONLY

# EXHIBIT FILED UNDER SEAL